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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/789,301	02/26/2004	Chul Hong Park	10031565-1	7633

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AGILENT TECHNOLOGIES, INC.  
Legal Department, DL429  
Intellectual Property Administration  
P.O. Box 7599  
Loveland, CO 80537-0599

EXAMINER

WILSON, ALLAN R

ART UNIT PAPER NUMBER

2815

DATE MAILED: 05/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

574

<b>Office Action Summary</b>	<b>Application No.</b> 10/789,301	<b>Applicant(s)</b> PARK, CHUL HONG	
	<b>Examiner</b> Allan R. Wilson	<b>Art Unit</b> 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 26 February 2004.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 16-20 is/are allowed.
- 6) ☒ Claim(s) 1,2,6-10,14 and 15 is/are rejected.
- 7) ☒ Claim(s) 3-5 and 11-13 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Claim Objections*

Claim 1 is objected to because of the following informalities: The term “increased” in claim 1 is a relative term which is confusing. Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 9 and 10 are rejected under 35 U.S.C. § 102(e) as being anticipated by Inokuchi et al. (“Inokuchi”) U.S. Patent No. 6,537,865.

With regards to claims 1 and 9, Inokuchi illustrates in figures 1-46, particularly figure 1, (entire document) a substrate 102; and a high electron mobility transistor formed on the substrate, the high electron mobility transistor including a source electrode 124, a drain electrode 126 and a gate electrode 150, the high electron mobility transistor having an increased gate-to-drain etch recess spacing, the increased gate-to-drain etch recess spacing providing a greater protection for the high electron mobility transistor from an electrostatic discharge on the drain electrode.

Art Unit: 2815

The First Embodiment disclose in col. 5, lines 34-36, gate-to-drain recess spacing of 1.5  $\mu\text{m}$  and the Sixteenth Embodiment discloses in col. 22, lines 21-23, gate-to-drain recess spacing of 0.6  $\mu\text{m}$ . Therefore, the First Embodiment will has "increased gate-to-drain etch recess spacing, the increased gate-to-drain etch recess spacing proving a greater protection for the high electron mobility transistor from an electrostatic discharge on the drain electrode" over the Sixteenth Embodiment.

With regards to claims 1 and 9, it would have been obvious for the limitation "proving a greater protection for the high electron mobility transistor from an electrostatic discharge on the drain electrode" since a device has the properties which meet the claimed limitation once the claimed materials and structure are present. Since the claimed material and structure limitation are met by Inokuchi, the limitation relating to the properties of the layers are also met as a natural result.

With regards to claims 2 and 10, Inokuchi discloses in at least col. 4, lines 56-58, the high electron mobility transistor includes an enhancement mode pseudomorphic high electron mobility transistor (PHEMT).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Art Unit: 2815

Claims 6, 7, 8, 14 and 15 are rejected under 35 USC § 103 (a) as being unpatentable over Inokuchi as applied to claims 1 and 9 above, and further in view of Higashisaka, U.S. Patent No. 5,030,852.

With regards to claims 6 and 14, Inokuchi is discussed above, it does not show a resistor formed over the substrate connected to the drain electrode of the high electron mobility transistor, the resistor being made of a semiconductor material. Higashisaka illustrates in figure 1 a resistor 3 formed over a substrate connected to the drain electrode of the high electron mobility transistor (col. 1, lines 21-23), the resistor being made of a semiconductor material. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a resistor for the objectives stated in Higashisaka col. 4, line 60 through col. 6, lines 47.

With regards to claims 7 and 15, Higashisaka illustrates in fig. 1 a reverse biased Schottky diode 6 formed over the substrate connected to the drain electrode of the high electron mobility transistor 1.

With regards to claim 8, the limitation “the reverse biased Schottky diode being configured to have an increased anode-to-cathode etch recess spacing to provide protection for the reverse biased Schottky diode from a positive electrostatic discharge” is an inherent function of the structure and since the prior art has the same structure and materials as the claimed invention it will have the same inherent function.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out

Art Unit: 2815

the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

***Allowable Subject Matter***

Claims 16-20 are allowable.

Claims 3-5 and 11-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Inokuchi et al., U.S. Patent No. 6,294,801 (illustrates a HEMT with a 26  $\mu\text{m}$  gate-to-drain spacing), Mishra et al. (illustrates a HEMT with a 2.5  $\mu\text{m}$  gate-to-drain spacing), Vaitkus (illustrates a heterojunction FET with a 10 to 20  $\mu\text{m}$  gate-to-drain spacing) and Maekawa et al. (illustrates a circuit with a resistor attached the a HEMT drain).

Field of Search	Date
U.S. Class and subclass: 257/192-195	May 5, 2005
Other Documentation: None	N/A
Electronic data base(s): EAST (USPAT, US-PGPUB, JPO, EPO, Derwent, IBM TDB)	May 5, 2005

Art Unit: 2815

Any inquiry concerning this communication or earlier communications from an examiner should be directed to Primary Examiner Allan Wilson whose telephone number is (571) 272-1738. Examiner Wilson can normally be reached 7:00-4:00 Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'A. Wilson', with a long horizontal flourish extending to the right.

Allan R. Wilson  
Primary Examiner  
May 5, 2005